Data Conversion and Lab (17.368)

Spring 2013

Lecture Outline

Class # 04

September 26, 2013

Dohn Bowden

Today's Lecture Outline

- Administrative
- Detailed Technical Discussions
  - Analog to Digital Conversion
- Lab
  - Finish Lab #2
  - Start Lab #3 (obtain parts and wire board for next week)
- Homework

Course Admin

Syllabus Review

Week	Date	Topics	Lab	Lab Report Due
1	09/05/13	Introduction/Basic Data Conversion, Course Overview, Op Amps in Data Conversion		
2	09/12/13	Op Amp Lab	1	
3	09/19/13	Sample and Hold Lecture and Lab	2	
4	09/26/13	A/D Conversion Fundamentals and Lab	3	1
5	10/03/13	A/D Conversion Lab Continuation	3 con't	
6	10/10/13	**Examination 1**		
7	10/17/13	D/A Conversion Fundamentals and Lab	4	2
8	10/24/13	D/A Conversion Lab Continuation		
9	10/31/13	Microcontroller and Sensors	4 con't	3
10	11/07/13	Microcontroller and Sensor Lab	5	
11	11/14/13	V/F and F/V Conversion Lecture	5 con't	4
12	11/21/13	**Examination 2**	Project	5
X	**11/28/13**	**No Class – Thanksgiving**		
13	12/05/13	Work on Course Project	Project	
14	12/12/13	Final Exam/Course Project Brief and Demonstration	Demo	

Class Hours

- Thursdays evenings ... 6:30 – 9:20 PM ...
    - **Lectures in BL-407????**
    - Labs will be in BL-407 ... (AFTER THE LECTURE)????

Detailed Technical Discussion

References …

References

- Lecture material is covered in the text as follows ...
  - Data Conversion Handbook
    - On line version (PDF)
      - Section 3.2, pages 3.39 – 3.103
      - Section 3.3, pages 3.109 – 3.133
    - Textbook (Hard Copy)
      - Pages 175 – 224
      - Pages 231 – 248

- **Continued next page ...**

References … continued

- “Understanding analog to digital converter specifications”, by Len Stellar. Embedded Systems Design, 02/24/05

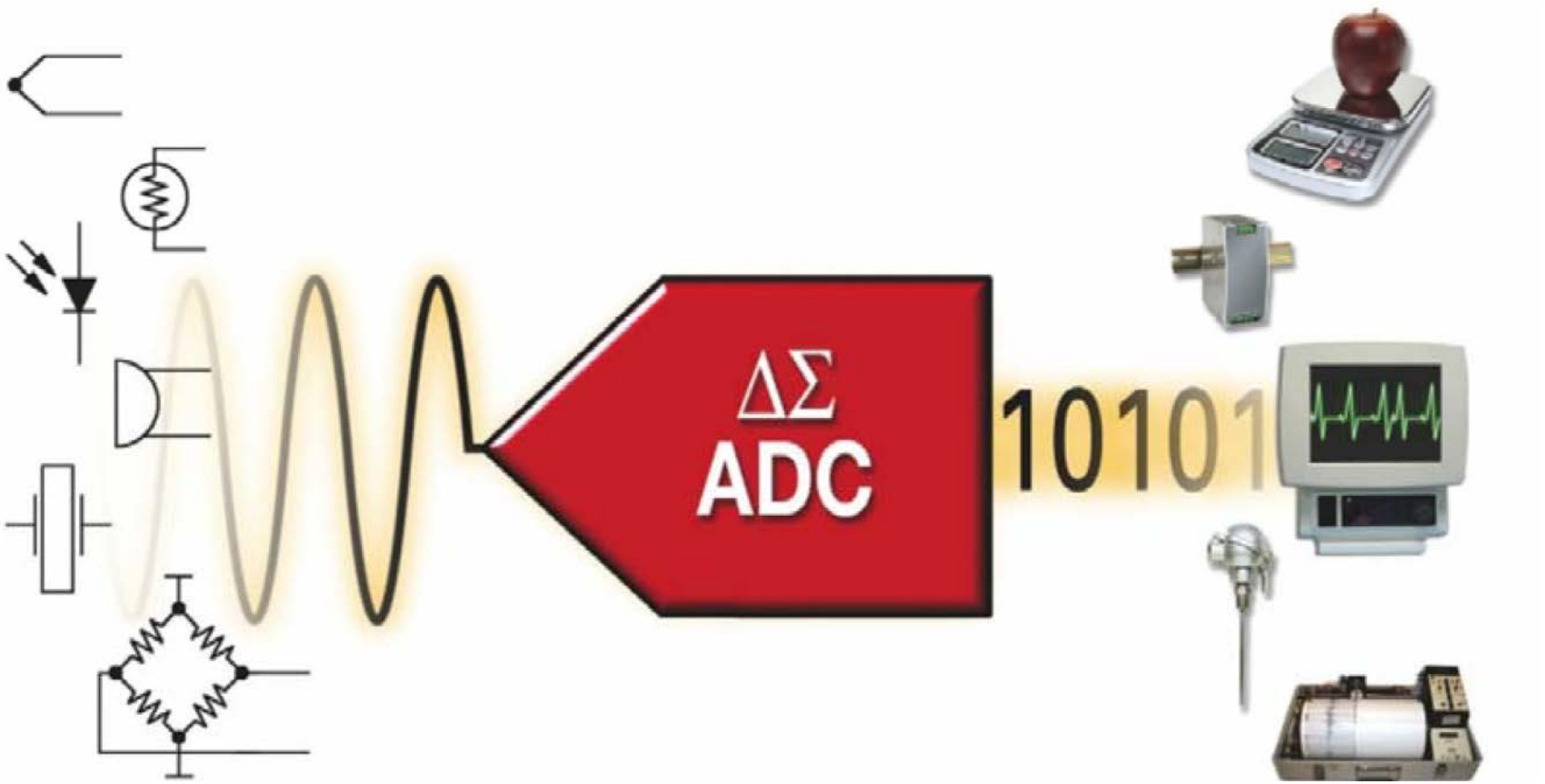
- Which ADC Architecture is Right for Your Application, by Walt Kester. Analog Dialogue 39-06, June 2005

- Freescale Semiconductor Application Note AN2438/D 2/2003

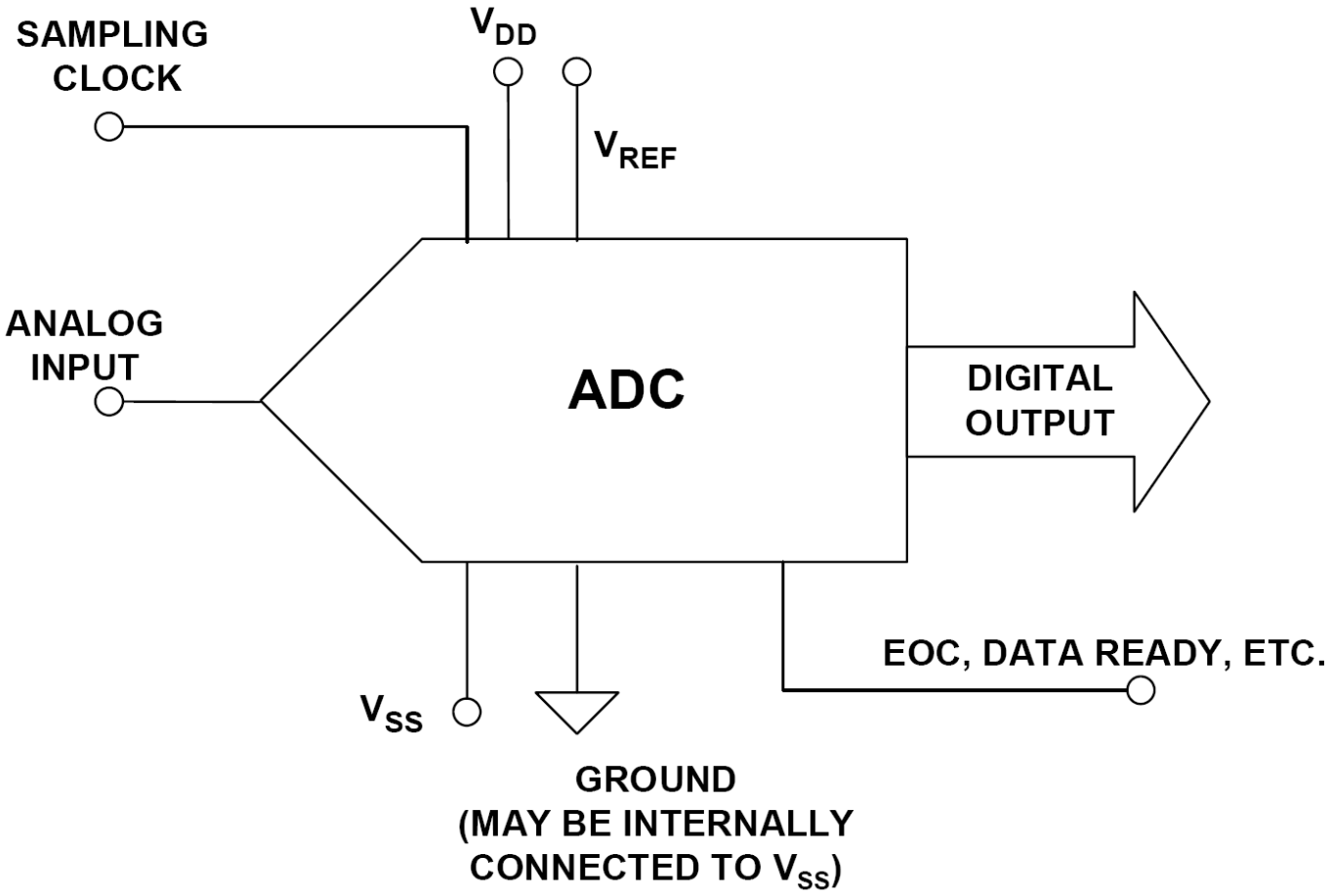
The above articles can be found on the class web page

ADC Overview …

Analog To Digital Conversion Overview



Basic ADC with External References



Analog To Digital Conversion Overview

- Analog to Digital conversion is a straight forward process
- We will be looking at the steps involved in the conversion
- We will look at the various architectures for ADCs

Sample and Hold …

Sample and Hold

- Use to be separate IC
  - Today ... most ADC include Sample and Hold circuitry
- Just because we don't see a separate Sample and Hold circuit ... does not mean we can ignore it!
- Recall ... the Sample and Hold circuit will hold the analog value constant during the Analog to Digital conversion process
  - If the analog signal changes half way through the process
    - Our conversion will be corrupt!

Sampling …

Sampling

- ***Sampling*** is ...
  - The reduction of a continuous signal to a discrete signal
  - Specifically ... ***Sampling*** is the process of analyzing the continuous analog signal with measurements taken at discrete and standard intervals
    - An example ... the conversion of a sound wave (a continuous-time signal) to a sequence of samples (a discrete-time signal)

How Often Do We Sample the Signal?

- We sample based on the *Nyquist* Criteria ... which is ...
  - A signal with a maximum frequency f_a must be sampled at a rate ...

$$f_s > 2f_a$$

  - ... Or information about the signal will be lost because of *aliasing*
    - » Where f_s is ... the sampling frequency
    - » And f_a is ... the maximum signal frequency

Simply Stated ...

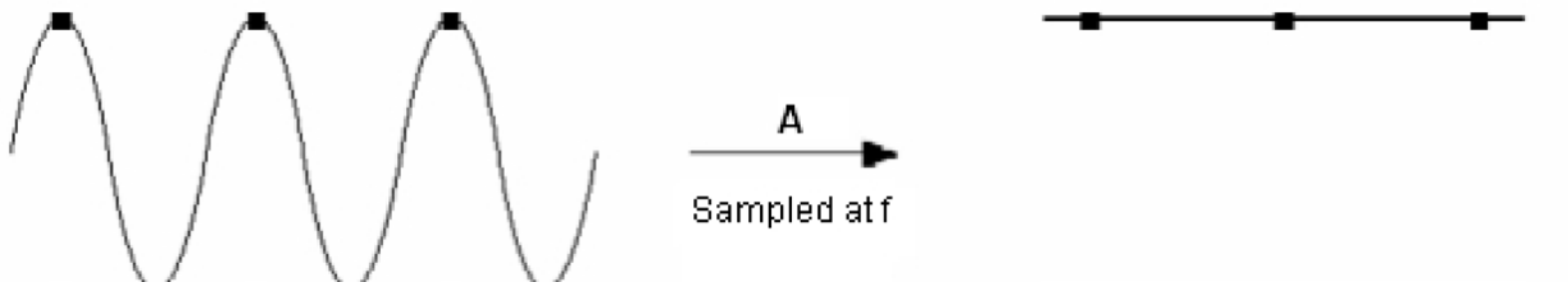
- The *Nyquist* criteria requires that the sampling frequency be ...
  - ... at least twice the highest frequency contained in the signal or information about the signal will be lost
- If the sampling frequency is less than twice the maximum analog signal frequency ...
  - a phenomena known as *aliasing* will occur

Aliasing

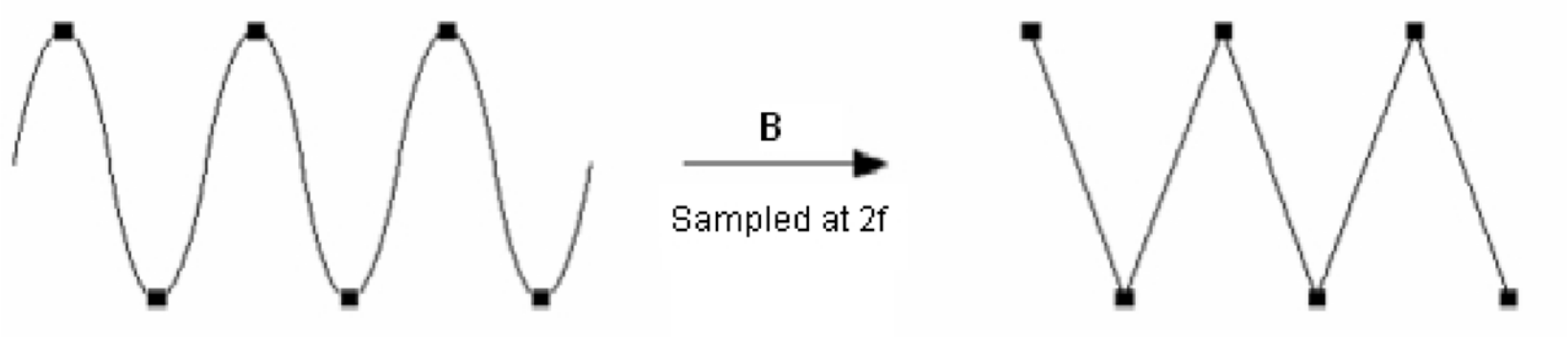
- ***Aliasing*** is the result of not sampling the analog signal at a high enough rate

- This will produce low-frequency signals (also called ***aliases***) that cannot be distinguished from the signal

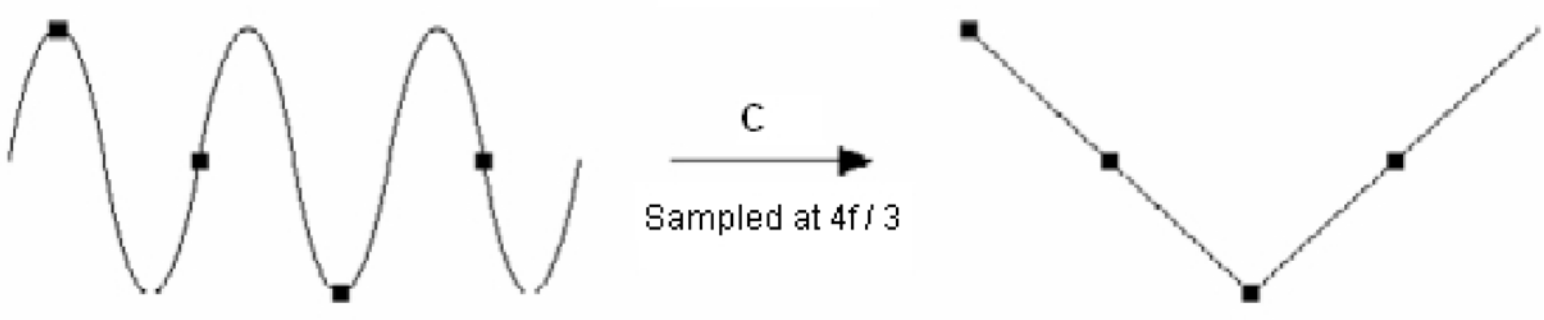
Sampling at f



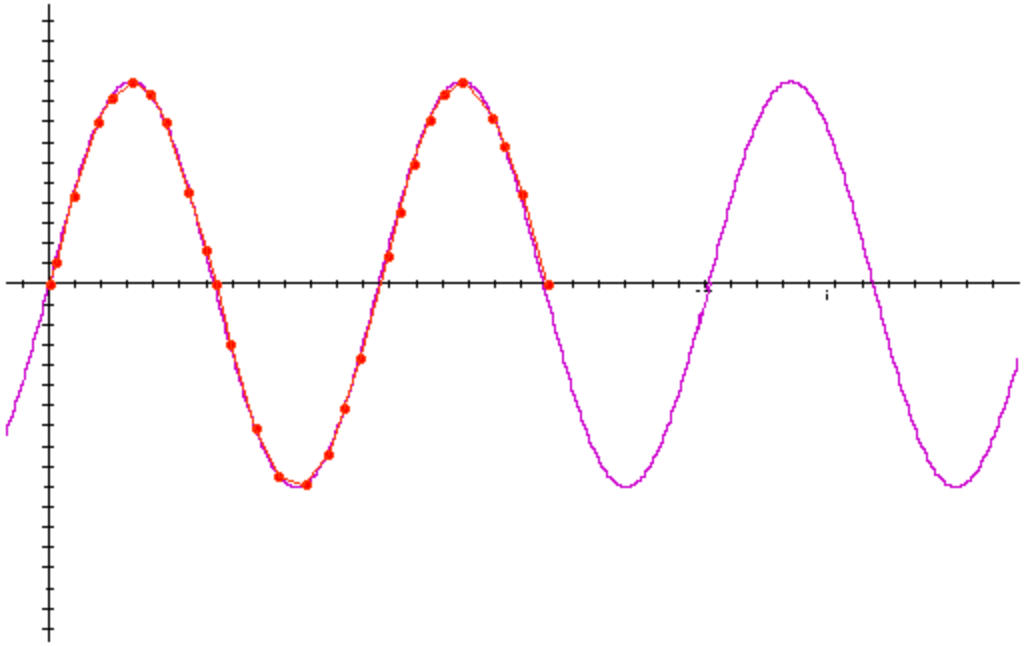
Sampling at 2f



Sampling at 4f / 3



Sampling at many times per cycle



Therefore ...

- As the sampling rate increases ...
  - The more signal values we gather to represent the analog signal
  - And you would think the more accurately you would represent the signal!
    - This is not true!

- It has been proven mathematically ...
  - That in order to reconstruct an analog signal from its sample points ...
    - All we need is to sample at a rate at least twice as fast as the highest frequency component of the signal

- This minimum sampling frequency ... known as the ***Nyquist Rate***

In Practice Sampling Rate ...

- In practice ... as a rule of thumb ...
  - We like to sample the analog signal at a rate ...

    5 to 10 times the highest frequency component

Quantization …

Quantization

- *Quantization* is ...
  - The procedure of constraining something from a continuous set of values (such as the real numbers) ...
  - ... to a discrete set (such as the integers)

Quantization

- The ADC represents an analog signal as a digital string of 1's and 0's with finite resolution
    - The ADC outputs a finite number of digital values ...
        - equal to 2^N

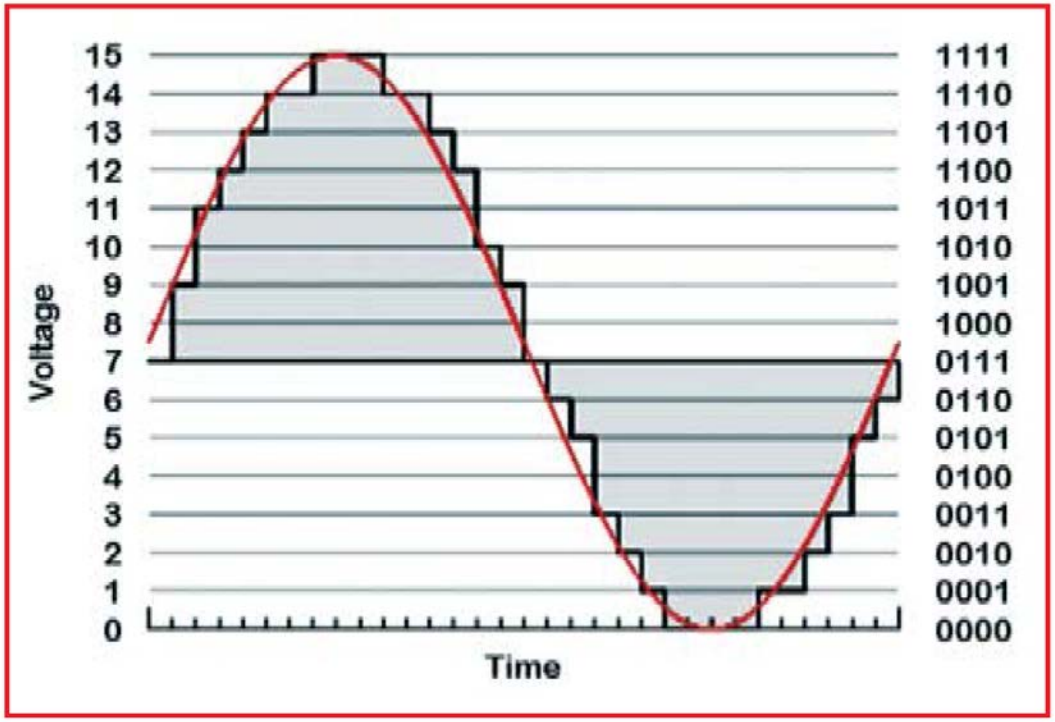
            (where N is the number of bits of the ADC)

Amplitude Quantization …

Amplitude Quantization

- *Amplitude Quantization:*
  - The maximum amplitude range of an analog signal must be divided into a fixed number of small, equal intervals
  - Each interval is then associated with a fixed binary number
    - The A/D Converter performs such a function
  - Factors that must be specific for an A/D Converter:
    - The maximum range of analog input voltage (Full Scale)
    - The output resolution (determined by the number of output bits)

Amplitude Quantization



Full Scale …

Full Scale

- ***Full Scale*** (FS) ...
  - The input range (span) of analog voltage accepted by the converter
    - (i.e. 0 to 10 volts)
- In converter technology ... ***Full Scale*** (FS) is independent of the number of bits of resolutions (N)
  - We will discuss bits of ***resolution*** (N) later

Resolution …

Resolution

- ***Resolution*** **...** Is a measure of the smallest change in analog input that can be discriminated by an A/D Converter
  - The more binary digits of output that are available ...
  - The more resolution that is possible, and ...
  - The more precision we can encode the analog signal
- The ***resolution*** of an 'N' bit A/D converter with a voltage range of "0 – X" volts is ...

$$\frac{X - 0}{2^N} \quad \text{or} \quad V_{step} = \frac{V_{\max} - V_{\min}}{2^N}$$

Example

- For a 4 bit converter
- Zero to fifteen volts input range
- We have

$$\frac{X - 0}{2^N} = \frac{15}{2^4} = \frac{15}{16} = 0.9375 \text{ per volt}$$

- The output of an A/D Converter is said to be accurate to within $\pm$ ½ LSB (Least Significant Bit)
- Hence, the accuracy of the above example would approximately be $\pm$ 0.47 V

Example

- For an 12-bit A/D Converter with a voltage range of 0 – 10 Volts, what would the resolution be?

$$\frac{10}{\left(2^{12}\right)} = \left(\frac{10}{4096}\right) = 2.44mV$$

Example

- Assume a voltage range of 0 – 10 Volts with a 14-bit A/D Converter ... what would the resolution be?

$$\frac{10}{\left(2^{14}\right)} = \left(\frac{10}{16{,}384}\right) = 0.61mV$$

- At this level of resolution, unavoidable noise of equal or greater amplitude generated within the analog circuitry of the A/D Converter would cause errors and signal information to be lost and not recoverable

Example

- For an 14-bit A/D Converter with FS voltage range (-10 to +10 Volts)

What is the resolution?

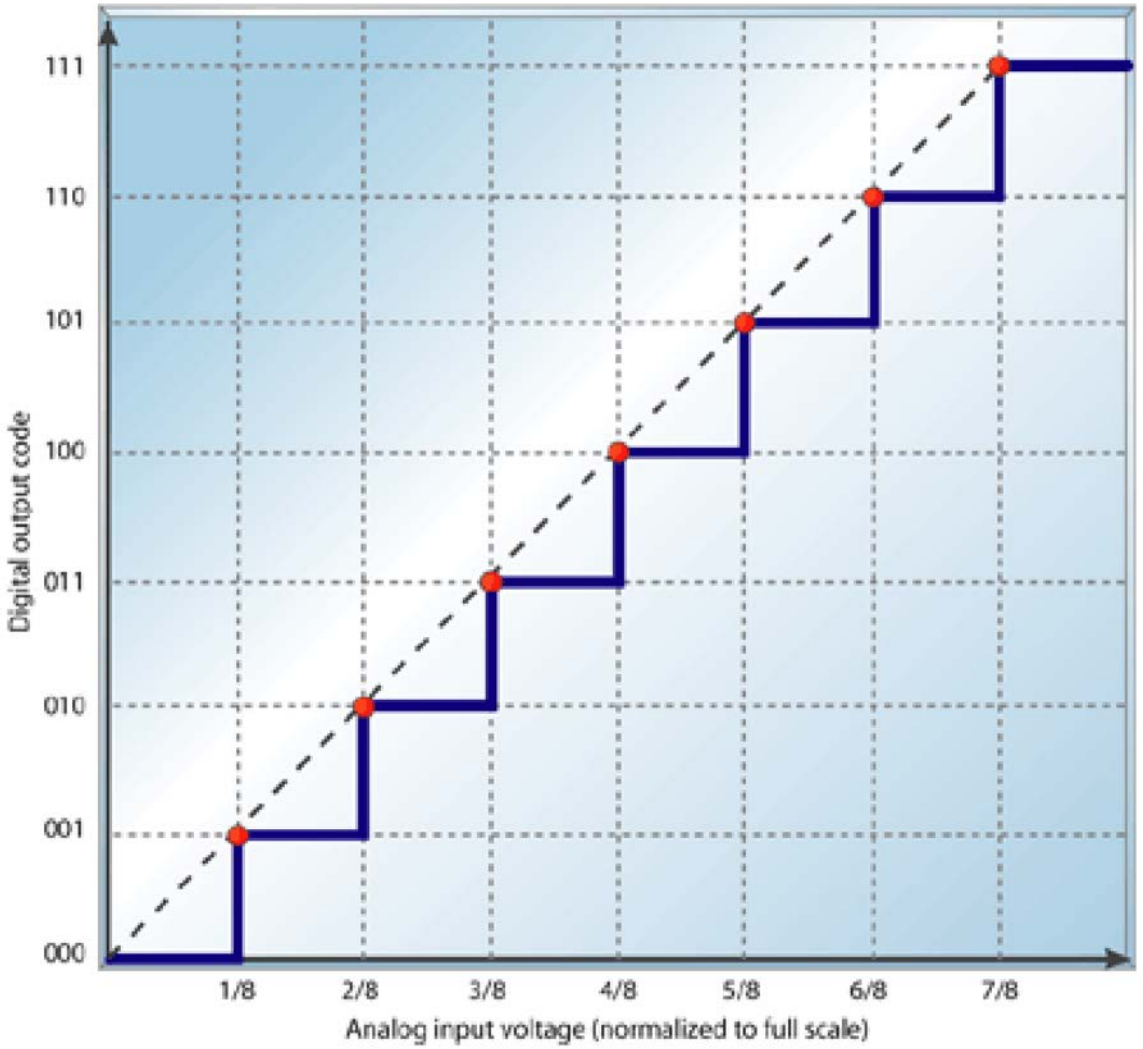
$$\frac{10-(-10)}{\left(2^{14}\right)}=\left(\frac{20}{16384}\right)=1.22mV$$

ADC Specifications …

ADC Specifications

- ADCs convert an analog signal input to a digital output code
- ADC measurements deviate from the ideal due to ...
  - Variations in the manufacturing process ... and ...
  - Through various sources of inaccuracy in the analog-to-digital conversion process
- The ADC performance specifications will quantify the errors that are caused by the ADC itself

Ideal transfer function of a 3-bit ADC



ADC Specifications

- ADC performance specifications are generally categorized in two ways ...
  - DC accuracy ... and ...
  - Dynamic performance

DC Accuracy

- Offset error
- Full-scale error
- Differential Nonlinearity (DNL)
- Integral Nonlinearity (INL)

Dynamic Performance

- Signal-to-noise ratio (SNR)
- Harmonic distortion
- Signal-to-noise and distortion (SiNAD)
- Spurious-free dynamic range

ADC Specifications

- For an in-depth look at ADC specifications ...
  - Read ...
    - "Understanding analog to digital converter specifications"

      by Len Stellar

      Embedded Systems Design, 02/24/05

      Link is on the course web site ...

ADC Architectures …

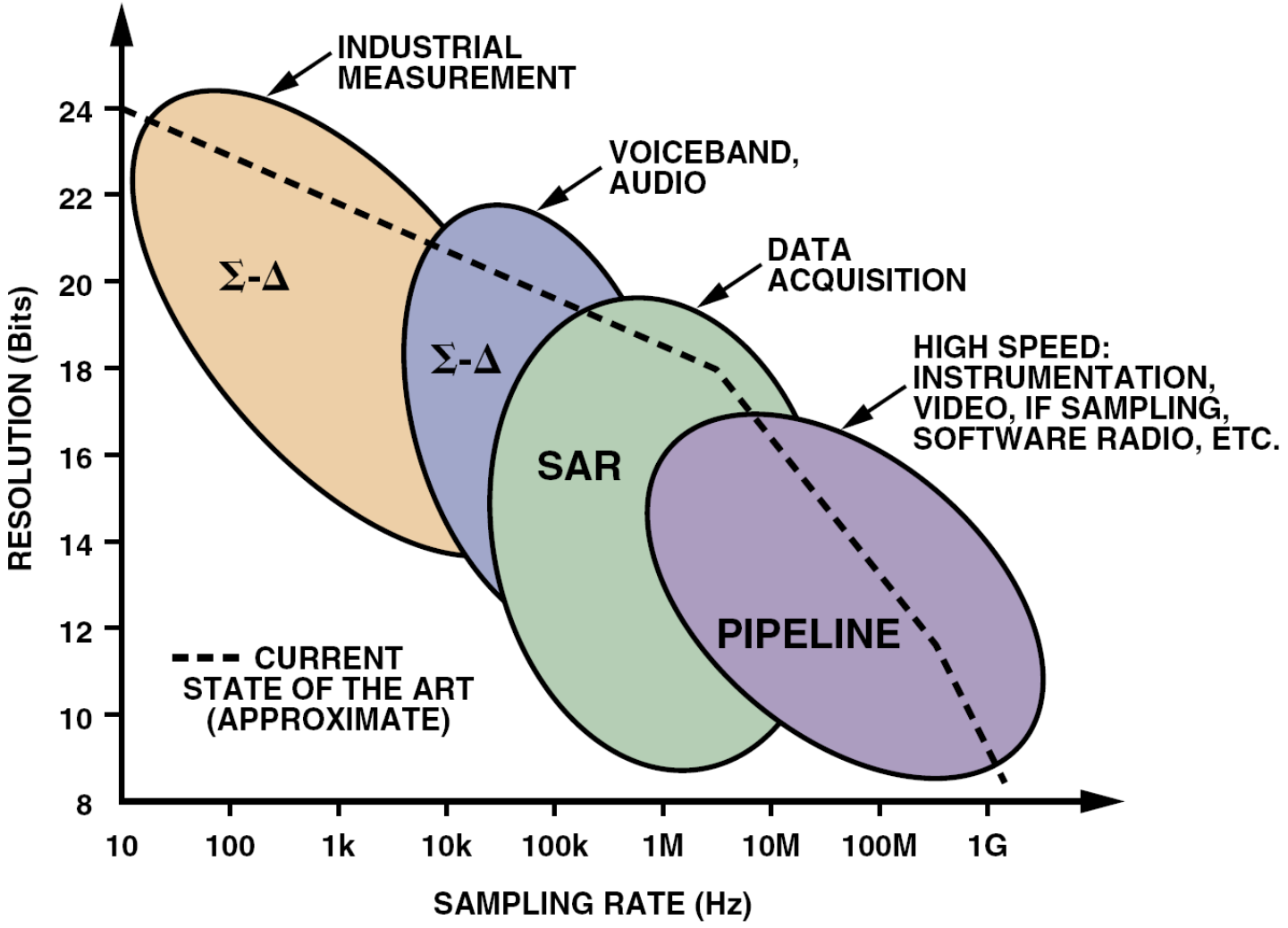
Analog to Digital Converter Architectures

- Most ADC applications today can be classified into four broad market segments:
  - Data acquisition
  - Precision industrial measurement
  - Voiceband and audio
  - “High speed”
    - Implying sampling rates greater than about 5 MSPS

Analog to Digital Converter Architectures

- A very large percentage of the previously stated applications can be filled by
  - Successive-approximation (SAR)
  - Sigma-delta (Σ-Δ)
  - Pipelined ADCs

ADC Architectures, Applications, Resolution, and Sampling Rates



Types of ADCs

- ADCs can be grouped into many different categories ...
    - Architecture type
    - Speed
    - Resolution
    - Power consumption

... to mention just a few

Successive Approximation Register (SAR) ADC…

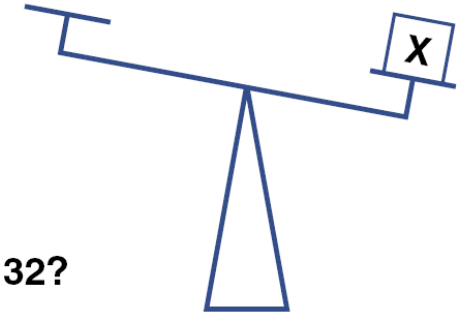
Successive-Approximation-Register or SAR ADC

- A **successive-approximation-register** or SAR ADC ...
  - Is more complex than some of the other ADC architectures
- But there are advantages to the complexity
  - The SAR ADC works by using a single comparator to compare the input analog voltage to an internal reference voltage for each bit in the conversion
    - Therefore ... the input signal needs to be compared ten times for an 10-bit resolution converter

Successive-Approximation-Register (con't)

- As each comparison takes place ...
    - a binary value of the approximation is stored in a register
- As comparisons and approximations continues ...
  - The register shifts to the next most significant bit until the word is complete
- This architecture is not the fastest ... but ...
  - It can provide an accurate approximation of the analog signal

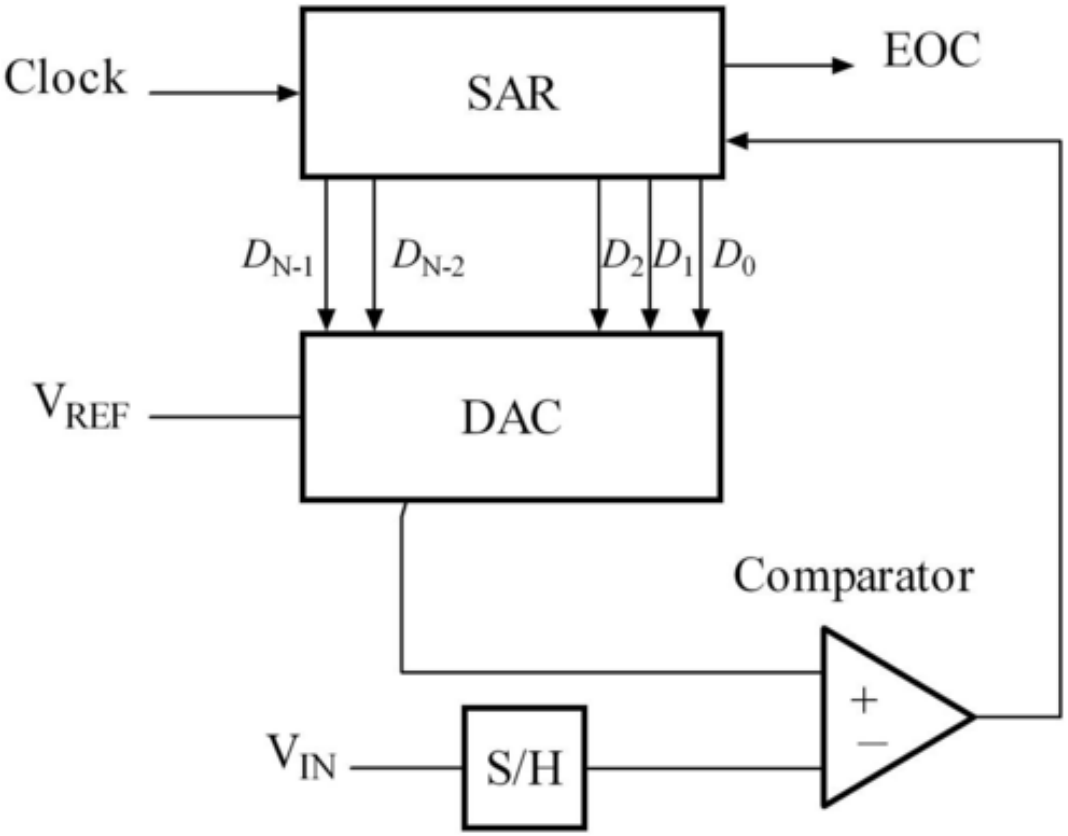
Successive Approximation ADC Algorithm



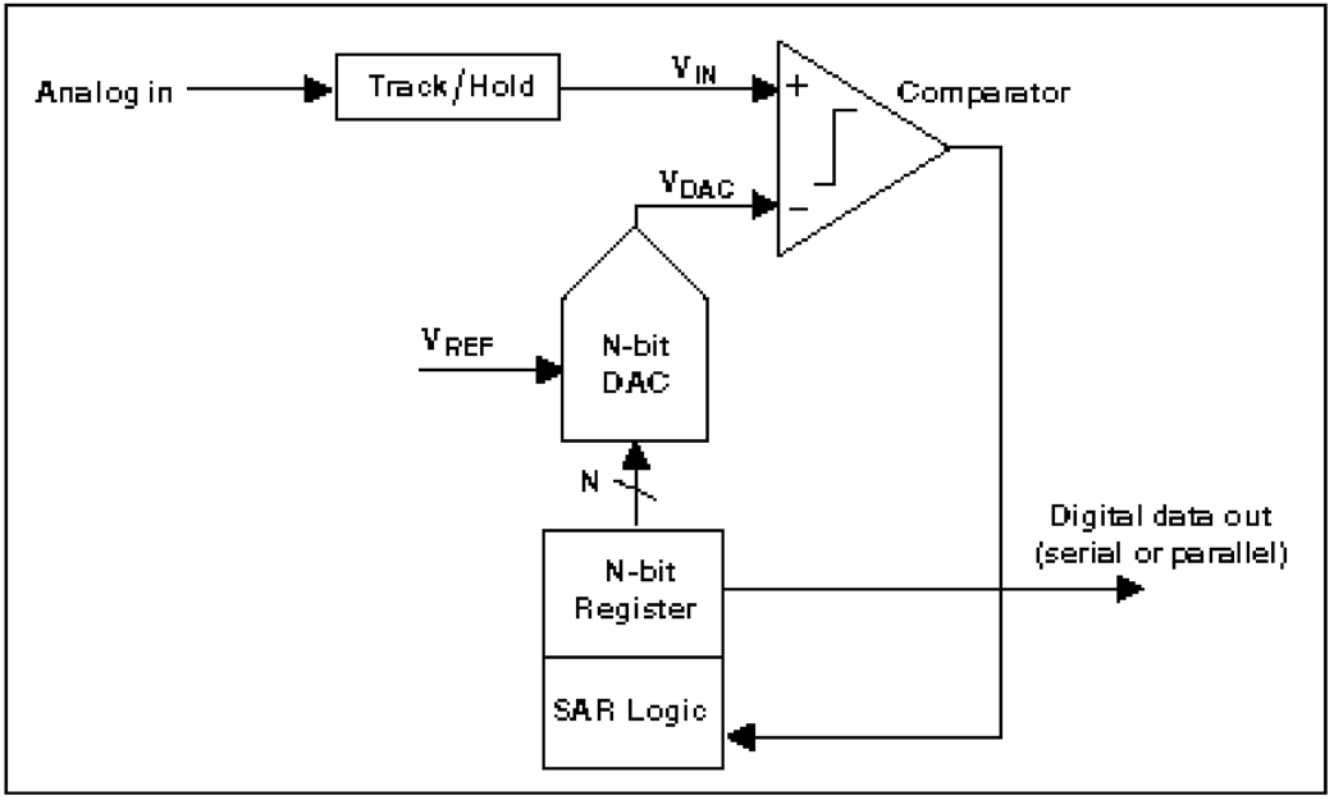
TEST	ASSUME X = 45
IS X $\geq$ 32?	YES $\rightarrow$ RETAIN 32 $\rightarrow$ 1
IS X $\geq$ (32 + 16)?	NO $\rightarrow$ REJECT 16 $\rightarrow$ 0
IS X $\geq$ (32 + 8)?	YES $\rightarrow$ RETAIN 8 $\rightarrow$ 1
IS X $\geq$ (32 + 8 + 4)?	YES $\rightarrow$ RETAIN 4 $\rightarrow$ 1
IS X $\geq$ (32 + 8 + 4 + 2)?	NO $\rightarrow$ REJECT 2 $\rightarrow$ 0
IS X $\geq$ (32 + 8 + 4 + 1)?	YES$\rightarrow$ RETAIN 1 $\rightarrow$ 1

TOTALS: X = 32 + 8 + 4 + 1 = 45_{10} = 101101_2

Successive Approximation ADC Block Diagram



Simplified N-bit SAR ADC architecture



Successive-Approximation-Register (SAR) ADC

- The SAR ADC circuit typically consists of four components:
  - A sample and hold circuit
  - An analog voltage comparator
    - Compares V_{in} to the output of the internal DAC
    - Results of the comparison goes to the register
  - A successive approximation register
    - Supplies an approximate digital code of V_{in} to the internal DAC
  - An internal reference DAC
    - Supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in}

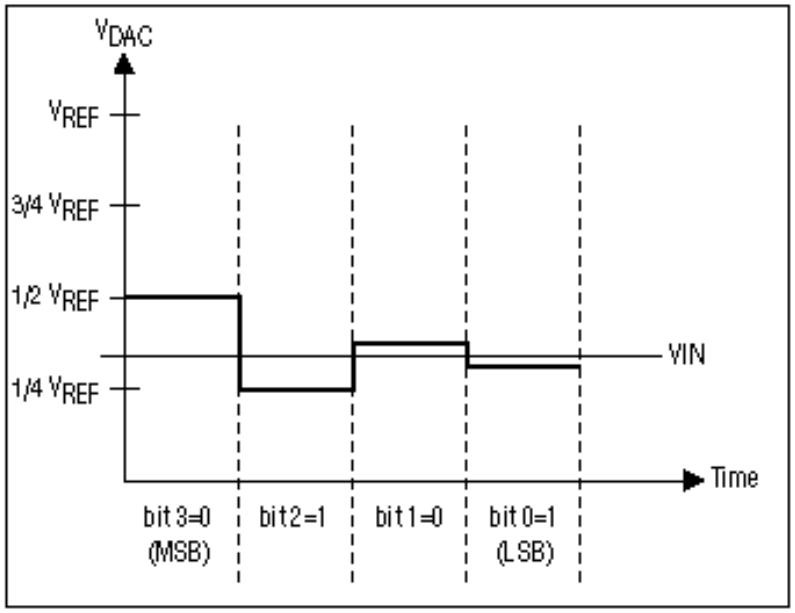
Successive Approximation ADC Algorithm

- The SAR is initialized so that the most significant bit (MSB) is equal to a digital 1
- The DAC supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage
- If this analog voltage exceeds Vin the comparator causes the SAR to reset this bit and set the next bit to a digital 1
- If it is lower then the bit is left a 1 and the next bit is set to 1

Successive Approximation ADC Algorithm (con't)

- This search continues until every bit in the SAR has been tested
- The result is the digital approximation of the sampled input voltage and ...
  - The digital value is provided by the ADC at the end of the conversion

Example --- 4-bit conversion



- The first comparison shows that $V_{IN} < V_{DAC}$
  - Bit 3 is set to '0'
  - The DAC is then set to 01002
- The second comparison is performed
  - $V_{IN} > V_{DAC}$ so bit 2 remains at '1'
  - The DAC is then set to 01102
- The third comparison is performed
  - Bit 1 is set to '0‘
  - The DAC is then set to 01012 for the final comparison
- Finally, bit 0 remains at '1' because $V_{IN} > V_{DAC}$

Sigma-Delta (Σ-Δ) …

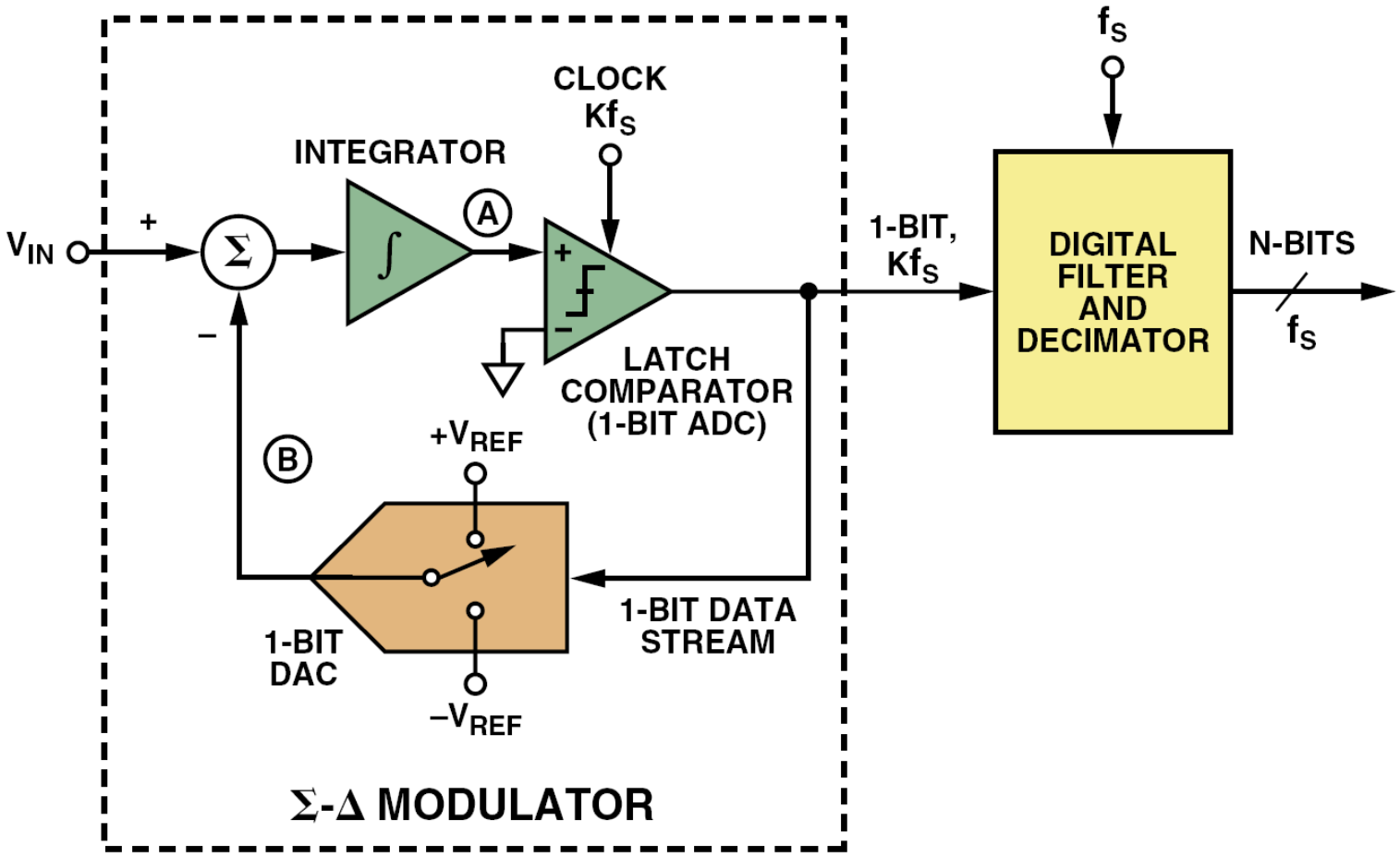
Sigma-Delta ADC

- **Sigma-Delta** (AKA ... Delta-Sigma) converters have relatively simple structures
  - a modulator
  - a digital decimation filter

- The modulator has ...
  - an integrator ... and ...
  - a comparator with a feedback loop that contains a 1-bit digital-to-analog converter

- The sigma-delta ADC also includes a clock that provides timing for the modulator and digital decimation filter

First-order Sigma-Delta ADC



Oversampling

- Sigma-delta converters use a technique called ***oversampling*** in order to achieve high-resolution outputs

- Oversampling is the process of ...
  - Sampling a signal with a sampling frequency significantly higher than twice the bandwidth or highest frequency of the signal being sampled.

- Oversampling
  - Reduces the sampling rate of the converter
  - And increases the ADC's resolution

Sigma-Delta ADC

- Sigma-delta converters are ...
  - Low cost
  - High resolution
- And can be incorporated into many system-on-chip designs

Pipelined ADCs …

Pipeline ADC

- The **pipeline** architecture is a variation on the flash ADC
- Therefore ...
  - A quick look at the Flash ADC ...

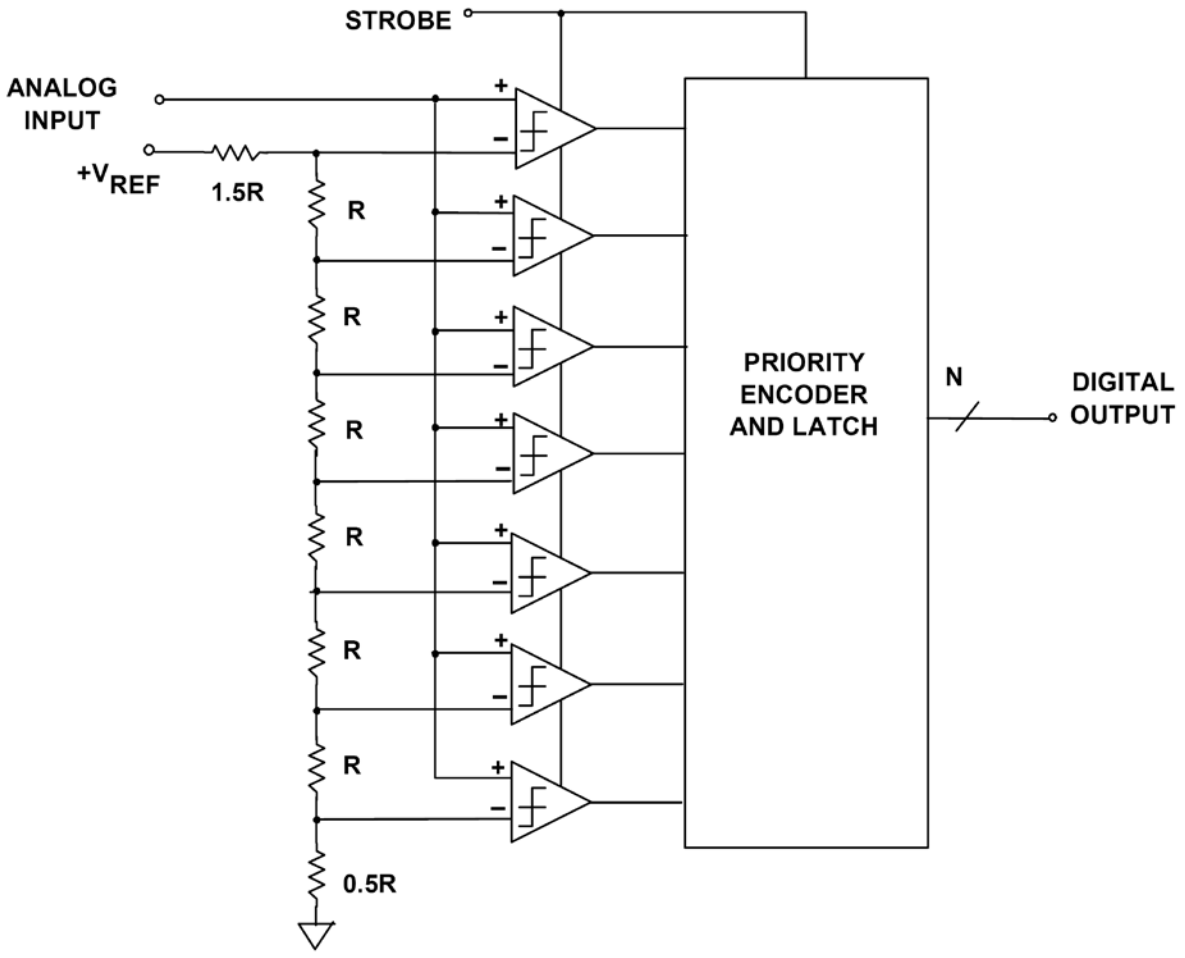
Flash ADCs

- Sometimes called direct conversion or parallel ADCs
- Uses comparators for each decoded voltage range
- The comparator bank feeds a logic circuit that generates a code for each voltage range

Flash ADCs

- Flash ADCs are the fastest converters on the market ...
  - ... but typically achieve only eight bits of resolution or less
- An 8-bit flash ADC would need 255 comparators in the circuit
  - This requires a large and expensive circuit
- Flash ADCs have a large die size ...
  - This in turn makes for high power consumption
- Flash ADCs are not the most accurate devices

3-bit Flash Converter



Pipeline ADC

- A pipelined ADC separates the process into several different processes that can be performed in a successive order
- Basically, three processes take place within the device ...
  - There is a sample-and-hold circuit
  - A flash ADC
  - And a digital-to-analog converter

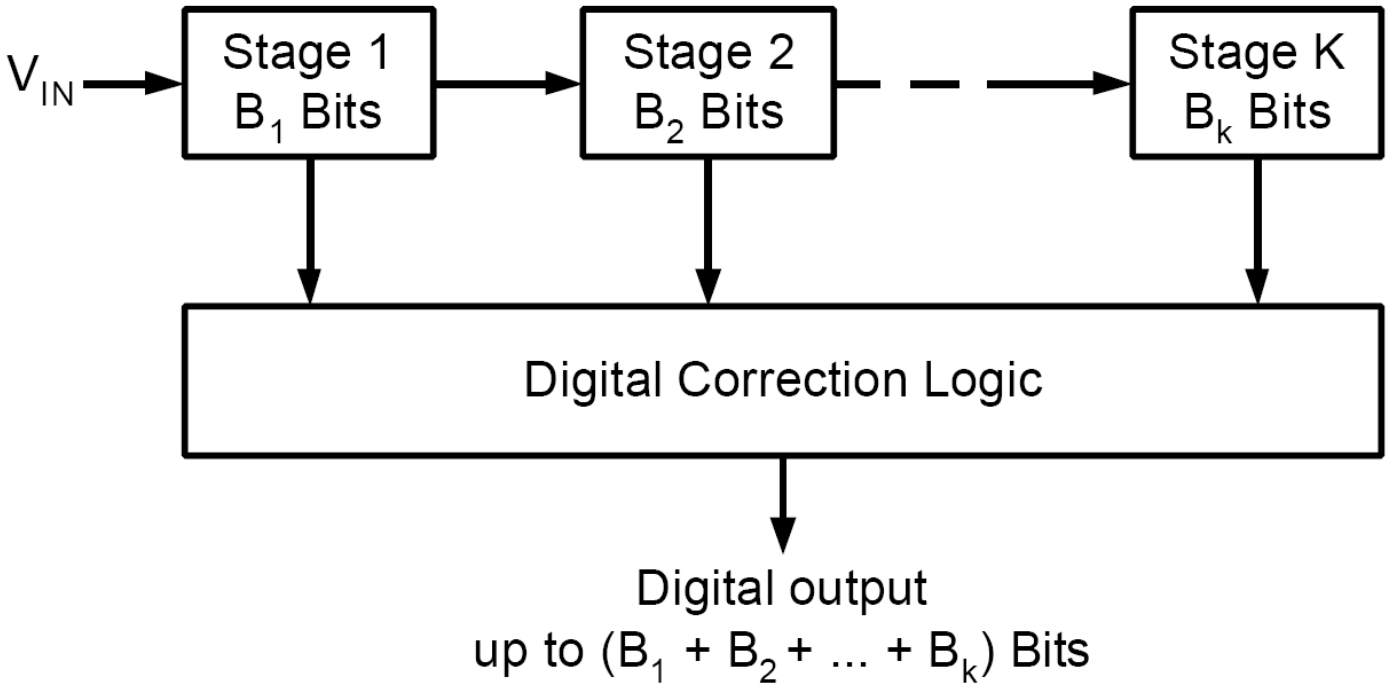
How the Pipeline process works

- The sample-and-hold circuit samples the analog input signal
- The flash converter converts the sample to a digital value
- The digital value becomes the most significant bits of the eventual digital output
- This digital value is then fed into a similar resolution digital-to-analog converter, and ...
  - ... The analog output signal is subtracted from the original analog signal
- The difference of the two analog signals is then ...
  - Amplified and inputted into the next stage of the pipeline to have the same process repeated as in the first stage
- This process continues until the desired resolution is obtained

Pipeline

- The resolution of the flash ADC and the DAC depend on the resolution of the pipelined ADC as a whole
- The pipelined ADC architecture is an alternative to the large size, power hungry flash ADC
- The pipeline ADC can offer ...
  - High resolution
  - And fast sampling rates
- But not as fast as the flash ADC

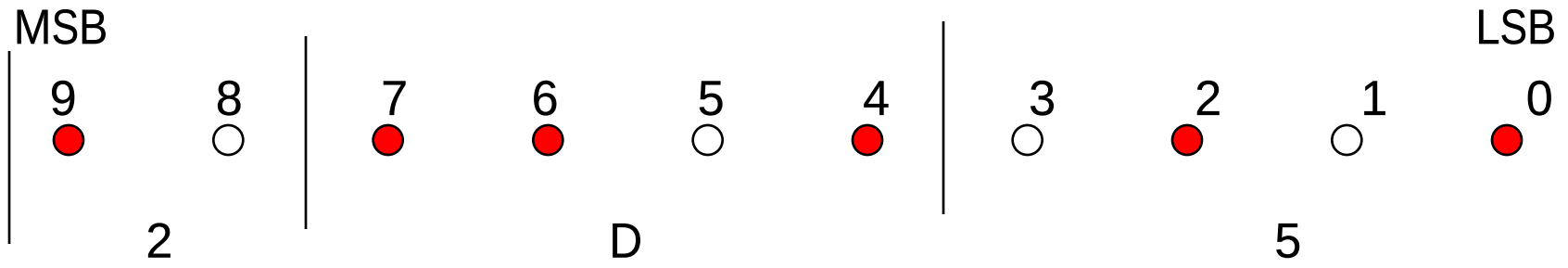
Pipeline ADC



ADCs Digital Output …

ADC Output

- LEDs (Digital) representation of Analog voltage ...

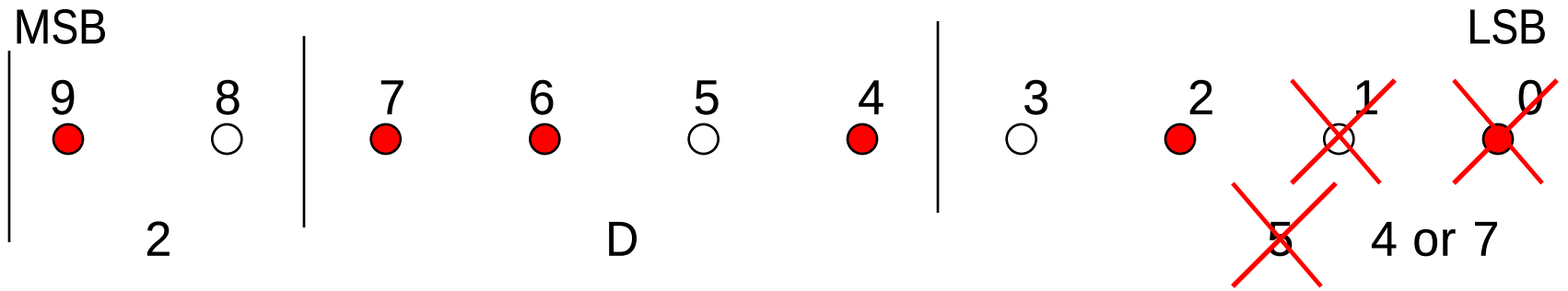


(###h)*(Vmax/2^N) = voltage 2D5h = 725_{10}

(2D5h)*(5/2^{10}) = 3.54 volts

ADC Output – Minus bits 0 and 1

- LEDs (Digital) representation of Analog voltage ...



(###h)*(Vmax/2^N) = voltage

2D4h = 724_{10}

2D7h = 727_{10}

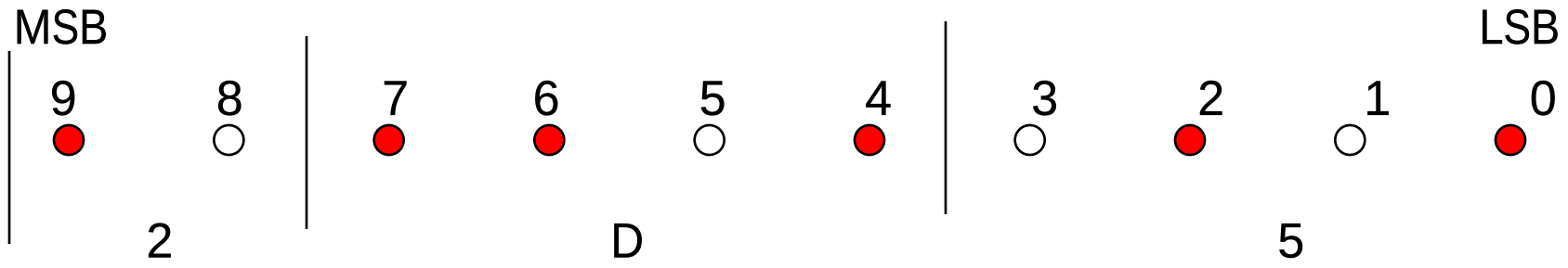
~~(2D5h)*(5/2^{10}) = 3.54 volts~~

(2D4h)*(5/2^{10}) = 3.53 volts

(2D7h)*(5/2^{10}) = 3.55 volts

ADC Output – another method

- LEDs (Digital) representation of Analog voltage ...



$(0bxxx)*(Vmax/2^N)$ = voltage

$(725_{10})*(5/2^{10})$ = 3.54 volts

$(2^0)*1$ =	1	$(2^5)*0$ =	0
$(2^1)*0$ =	0	$(2^6)*1$ =	64
$(2^2)*1$ =	4	$(2^7)*1$ =	128
$(2^3)*0$ =	0	$(2^8)*0$ =	0
$(2^4)*1$ =	16	$(2^9)*1$ =	512
			725

Table 1 – ADC804 Datasheet

TABLE 1. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR MS GROUP	FRACTIONAL BINARY VALUE FOR LS GROUP	OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560\ V_{DC}$ VMS GROUP (Note 15)	OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2=2.560\ V_{DC}$ VLS GROUP (Note 15)
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2.880	0.180
8	1	0	0	0	1/2	1/32	2.560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1.280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

Note 15: Display Output=VMS Group + VLS Group

Lab

Lab #3 ...

Lab #3– Overview

- To construct and operate an A/D Converter using the ADC804

Next Class

Next Class Topics

- Start/Finish Lab #3

Homework

Homework

1. Lab Reports – Lab report #2 is due 10/17/13

2. Read the following ...

   – The text ...

      – Pages 175 – 224 ... on-line Section 3.2, pages 3.39 – 3.103

      – Pages 231 – 248 ... on-line Section 3.3, pages 3.109 – 3.133

   – "Understanding analog to digital converter specifications", by Len Stellar. Embedded Systems Design, 02/24/05

   – Which ADC Architecture is Right for Your Application, by Walt Kester. Analog Dialogue 39-06, June 2005

   – Freescale Semiconductor Application Note AN2438/D 2/2003

The above articles can be found on the class web page

Time to start the lab …

Lab

- Finish Lab #2 ... Start Lab #3

Questions?

References ...

References

1. See within